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10/724,040	12/01/2003	Naoki Matsunaga	Q76864	1459

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,040	MATSUNAGA ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *20 and 21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1203*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 12/01/2003 through 10/25/2005.

Claims 1-21 are active in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

a. Information Disclosure Statement (IDS) filed on 12/01/2003. The references cited on the PTOL 1449 form have not been considered because no (abstract) translation(s) of the foreign documents being provided.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

b. Applicant made a provisional election without traverse to prosecute the invention of Group I, claims 1-19, drawn to semiconductor device(s) in the Response to Restriction Requirement filed 10/25/2005.

Claims 20-21 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected group there being no allowable generic or linking claim.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

Foreign Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

4. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication No. 2003/0025848 to Sera et al.

The applied reference has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Sera discloses a thin film transistor, as shown in figs. 5-24, comprising:

an active layer 7, in which a source region 7a and drain region 7e are formed;

a first light-shielding film 3 shielding a light incident on said active layer 7; and

a second light-shielding film 5 disposed between said active layer 7 and said first light-shielding film 3, wherein a carrier concentration of at least a surface portion of said second light-shielding film which opposes said active layer is about $10^{17}/cm^3$ or less. See also paragraphs [0136-0137], [0148-0159], [0173-0183], and [0246-0249].

Regarding claim 2, Sera discloses the thin film transistor wherein a distance between said second light-shielding film and said active layer is from about 100 nm to about 350 nm. See paragraphs [0169-0170].

Regarding claim 3, Sera discloses the thin film transistor wherein said active layer 7 has a low-concentration carrier region 7b/7d between a source region 7a and a channel region 7c, and wherein between a drain region 7e and the channel region 7c, said low-concentration carrier region has the same conductive type as the source region and the drain region and has lower impurity concentration than the source region and the drain region, and wherein said second light-shielding film 5 has a portion which overlaps said channel region and said low-concentration carrier region in terms of plane. See figs. 5, and paragraphs [0155-0159].

Regarding claim 4, Sera discloses the thin film transistor wherein said second light-shielding film 5 has a photo-absorption property. See paragraph [0048].

Regarding claim 5, Sera discloses the thin film transistor further comprising a dielectric film 4 disposed between said first light-shielding film and said second light-shielding film. See figs. 5.

Regarding claim 6, Sera disclose the thin film transistor wherein said second light-shielding film is formed on said first light-shielding film. See figs. 5.

Regarding claim 7, Sera discloses a thin film transistor layer, as shown in figs. 5-24, comprising:

an active layer, in which a source region 7a and drain region 7e are formed;

a first light-shielding film 3 shielding a light incident on said active layer 7; and

a second light-shielding film 5 disposed between said active layer 7 and said first light-shielding film 3, wherein an electric field intensity of a surface portion of said second light-shielding film which opposes said active layer includes about 80% or less of that of a surface portion of said second light-shielding film which opposes said first light-shielding film. See also paragraphs [0136-0137], [0148-0159], [0173-0183], and [0246-0249]. It is further noted that the surface portion of the second light-shielding film can obviously and varyingly be chosen, therefore the electric field intensity of the chosen portion can also be varied, and definitely be able to have value of about 80% or less of that of the surface portion of the second light shielding film.

Regarding claim 8, Sera discloses the thin film transistor wherein a distance between said second light-shielding film and said active layer is from about 100 nm to about 350 nm. See paragraphs [0169-0170].

Regarding claim 9, Sera discloses a thin film transistor, as shown in figs. 5-24, comprising:

an active layer 7, in which a source region 7a and drain region 7e are formed;

a first light-shielding film 3 shielding a light incident on said active layer; and

a second light-shielding film 5 disposed between said active layer and said first light-shielding film, wherein said second light-shielding film is made of a semi-insulating film. See also paragraphs [0136-0137], [0148-0159], [0173-0183], and [0246-0249].

Regarding claim 10, Sera discloses the thin film transistor wherein a carrier concentration of said second light-shielding film is about $10^{17}/cm^3$ or less. See also paragraphs [0136-0137], [0148-0159], [0173-0183], and [0246-0249].

Regarding claim 11, Sera discloses a thin film transistor, as shown in figs. 5-24, comprising:

an active layer 7, in which a source region 7a and drain region 7e are formed;

a first light-shielding film 3 shielding a light incident on said active layer;

a second light-shielding film 5 disposed between said active layer 7 and said first light-shielding film 3, wherein said second light-shielding film 5 is made of a material selected from a group consisting of amorphous silicon, crystallite silicon, amorphous Silicon Germanium, poly germanium, amorphous germanium, poly Silicon Germanium, and any combination thereof. See also paragraphs [0136-0137], [0148-0159], [0173-0183], and [0246-0249].

Regarding claim 12, Sera discloses the thin film transistor wherein a carrier concentration of said second light-shielding film is about 10.sup.17/cm.sup.3 or less. See also paragraphs [0136-0137], [0148-0159], [0173-0183], and [0246-0249].

Regarding claim 13, Sera discloses a thin film transistor substrate, as shown in figs. 5-24, comprising:

a light transmission substrate 1;

a transistor array including a plurality of thin film transistors disposed on said light transmission substrate 1;

a first light-shielding film 3 disposed between said light transmission substrate 1 and at least one of said thin film transistors;

a second light-shielding film 5 disposed between said first light-shielding film 3 and an active layer 7 of said thin film transistor, wherein a carrier concentration of a surface portion of said second light-shielding film which opposes said active layer is about $10^{17}/cm^3$ or less. See also paragraphs [0136-0137], [0148-0159], [0173-0189], and [0246-0249].

Regarding claim 14, Sera discloses the thin film transistor substrate further comprising pixel electrodes 15 corresponding to each of said plurality of thin film transistors, wherein each of said pixel electrode 15 is driven by a thin film transistor which said pixel electrode corresponds to. See paragraphs [0180-0190].

Regarding claim 15, Sera discloses the thin film transistor substrate wherein a dielectric film inbetween capacitance electrodes is connected to said pixel electrodes in parallel. See figs. 5.

Regarding claim 16, Sera discloses the thin film transistor substrate further comprising another thin film transistor which comprises neither said first light-shielding film nor said second light-shielding film. See fig. 26 and paragraphs [0243-0249].

Regarding claim 17, Sera discloses the thin film transistor substrate wherein an electric field intensity of a surface portion of said second light-shielding film which opposes said active layer includes about 80% or less of that of a surface portion of said second light-shielding film which opposes said first light-shielding film. It is noted that the surface portion of the second light-shielding film can obviously and varyingly be chosen, therefore the electric field intensity of the chosen portion can also be varied, and definitely be able to have value of about 80% or less of that of the surface portion of the second light shielding film.

Regarding claim 18, Sera discloses the thin film transistor substrate wherein said second light-shielding film is made of a material selected from a group consisting of amorphous silicon, crystallite silicon, amorphous Silicon Germanium, poly germanium, amorphous germanium, poly Silicon Germanium, and any combination thereof. See also paragraphs [0136-0137], [0148-0159], [0173-0183], and [0246-0249].

Regarding claim 19, Sera discloses the liquid crystal display unit comprising:

a thin film transistor substrate 1;

an opposite substrate disposed to oppose said thin film transistor substrate; and

a liquid crystal layer disposed between said thin film transistor substrate and said opposite substrate. See paragraphs [0136-0137], [0148-0159], [0173-0189], and [0246-0249].

7. Claim(s) 7-9 and 11 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. U.S. Patent No. 6,912,020 to Kawata; or by U.S. Patent Application Publication No. 2002/0071072 by Ohtani et al.

Regarding claim 7, Kawata discloses a thin film transistor, as shown in figs. 1-7 and 15, comprising:

an active layer 1a, in which a source region 1d and drain region 1e are formed; a

first light-shielding film M1 (or B4/M5/M6 (figs. 3-7)) shielding a light incident on said active layer 1a; and

a second light-shielding film B1 (or B3/M4) disposed between said active layer and said first light-shielding film, wherein an electric field intensity of a surface portion of said second light-shielding film which opposes said active layer includes about 80% or less of that of a surface portion of said second light-shielding film which opposes said first light-shielding film.

Alternately, still with regard to claim 7, Ohtani discloses a thin film transistor, as shown in figs. 5-10, comprising:

an active layer 605/606/608, in which source/drain regions 617 are formed;

a first light-shielding film 601 shielding a light incident on said active layer; and

a second light-shielding film 603 disposed between said active layer and said first light-shielding film 601, wherein an electric field intensity of a surface portion of said second light-shielding film which opposes said active layer includes about 80% or less of that of a surface portion of said second light-shielding film which opposes said first light-shielding film.

It is noted that the surface portion of the second light-shielding film can obviously and varyingly be chosen, therefore the electric field intensity of the chosen portion can also be varied, and definitely be able to have value of about 80% or less of that of the surface portion of the second light shielding film.

Regarding claim 8, Kawata/Ohtani discloses the thin film transistor wherein a distance between said second light-shielding film and said active layer is from about 100 nm to about 350 nm. See paragraph [0041] of Ohtani.

Regarding claim 9, Kawata discloses a thin film transistor, as shown in figs. 1-7 and 15, comprising:

an active layer 1a, in which a source region 1d and drain region 1e are formed;

a first light-shielding film M1 (or B4/M5/M6 (figs. 3-7)) shielding a light incident on said active layer; and

a second light-shielding film B1 (or B3/M4) disposed between said active layer and said first light-shielding film, wherein said second light-shielding film is made of a semi-insulating film. See col. 16, line 12 to col. 17, line 36; and col. 19, line 65 to col. 21, line 2.

Alternately, with regard to claim 9, Ohtani discloses a thin film transistor, as shown in figs. 5-10, comprising:

an active layer 605/606/608, in which source/drain regions 617 are formed;

a first light-shielding film 601 shielding a light incident on said active layer; and

a second light-shielding film 603 disposed between said active layer and said first light-shielding film 601, wherein said second light-shielding film is made of a semi-insulating film. See paragraphs [0040]-[0044].

Regarding claim 11, Kawata discloses a thin film transistor, as shown in figs. 1-7 and 15, comprising:

an active layer 1a, in which a source region 1d and drain region 1e are formed;

a first light-shielding film M1 (or B4/M5/M6 (figs. 3-7)) shielding a light incident on said active layer;

a second light-shielding film B1 (or B3/M4) disposed between said active layer and said first light-shielding film, wherein said second light-shielding film is made of a material selected from a group consisting of amorphous silicon, crystallite silicon, amorphous Silicon Germanium, poly germanium, amorphous germanium, poly Silicon

Germanium, and any combination thereof. See col. 16, line 12 to col. 17, line 36; and col. 19, line 65 to col. 21, line 2.

Alternately, with regard to claim 11, Ohtani discloses a thin film transistor, as shown in figs. 5-10, comprising:

an active layer 605/606/608, in which source/drain regions 617 are formed;

a first light-shielding film 601 shielding a light incident on said active layer;

a second light-shielding film 603 disposed between said active layer and said first light-shielding film, wherein said second light-shielding film 603 is made of a material selected from a group consisting of amorphous silicon, crystallite silicon, amorphous Silicon Germanium, poly germanium, amorphous germanium, poly Silicon Germanium, and any combination thereof. See paragraphs [0040]-[0044].

Claim Rejections - 35 U.S.C. § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim(s) 1-6, 10, and 12-19 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,912,020 to Kawata, or over U.S. Patent Application Publication No. 2002/0071072 by Ohtani et al., in view of the following remarks.

Regarding claims 1, Kawata discloses a thin film transistor, as shown in figs. 1-7 and 15, comprising:

an active layer 1a, in which a source region 1d and drain region 1e are formed;

a first light-shielding film M1 (or B4/M5/M6 (figs. 3-7)) shielding a light incident on said active layer 1a; and

a second light-shielding film B1 (or B3/M4) disposed between said active layer 1a and said first light-shielding film.

Alternately, with regard to claim 1, Ohtani discloses a thin film transistor, as shown in figs. 5-10, comprising:

an active layer 605/606/608, in which source/drain regions 617 are formed;

a first light-shielding film 601 shielding a light incident on said active layer 505; and

a second light-shielding film 603 disposed between said active layer 605/606/608 and said first light-shielding film 601.

Kawata and/or Ohtani is/are not necessary discuss about the carrier concentration of the second light shielding film because it would have been obvious to one having ordinary skill in the art at the time the invention was made that the carrier

concentration of the second light-shielding film of Kawata and/or Ohtani can be chosen at various value(s), and at least one of such values can be in the range of $10^{17}/cm^3$ or less (since this is a wide range), since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233; or that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). See also paragraphs [0054-0069] of Ohtani.

Regarding claims 2, Kawata/Ohtani discloses the thin film transistor wherein a distance between said second light-shielding film and said active layer is from about 100 nm to about 350 nm. See paragraph [0041] of Ohtani.

Regarding claim 3, Kawata/Ohtani discloses the thin film transistor wherein said active layer has a low-concentration carrier region between a source region and a channel region, and wherein between a drain region and the channel region, said low-concentration carrier region has the same conductive type as the source region and the drain region and has lower impurity concentration than the source region and the drain region, and wherein said second light-shielding film has a portion which overlaps said channel region and said low-concentration carrier region in terms of plane. See figs. 3, 15 of Kawata, or figs. 7e-9 of Ohtani.

Regarding claim 4, Kawata/Ohtani discloses the thin film transistor wherein said second light-shielding film has a photo-absorption property. See col. 11, line 17 to col. 12, line 52; col. 16, line 50 to col. 17, line 36.

Regarding claim 5, Kawata/Ohtani discloses the thin film transistor further comprising a dielectric film 12 (fig. 3, 15 of Kawata) or 602 (figs. 6-9 of Ohtani) disposed between said first light-shielding film and said second light-shielding film.

Regarding claim 6, Kawata/Ohtani discloses the thin film transistor wherein said second light-shielding film is formed on said first light-shielding film. See figs. 3, 15 of Kawata, or figs. 6-9 of Ohtani.

Regarding claims 10 and 12, Kawata and/or Ohtani disclose(s) the thin film transistor comprising all claimed limitations. Note that Kawata and/or Ohtani is/are not necessary discuss about the carrier concentration of the second light shielding film because it would have been obvious to one having ordinary skill in the art at the time the invention was made that the carrier concentration of the second light-shielding film of Kawata and/or Ohtani can be chosen at various value(s), and at least one of such values can be in the range of $10^{17}/cm^3$ or less (since this is a wide range), since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233; or that discovering an optimum value of a result effective variable

involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). See also paragraphs [0054-0069] of Ohtani.

Regarding claim 13, Kawata discloses a thin film transistor substrate, as shown in figs. 1-7 and 15, comprising:

a light transmission substrate 10;

a transistor array including a plurality of thin film transistors disposed on said light transmission substrate 10;

a first light-shielding film M1 (or B4/M5/M6 (figs. 3-7)) disposed between said light transmission substrate 10 and at least one of said thin film transistors;

a second light-shielding film (or B3/M4) disposed between said first light-shielding film and an active layer of said thin film transistor.

Alternately, with regard to claim 13, Kawata discloses a thin film transistor substrate, as shown in figs. 5-10, comprising:

a light transmission substrate 600;

a transistor array including a plurality of thin film transistors disposed on said light transmission substrate 600;

a first light-shielding film 601 disposed between said light transmission substrate 600 and at least one of said thin film transistors;

a second light-shielding film 603 disposed between said first light-shielding film and an active layer 605/606/608 of said thin film transistor.

Kawata and/or Ohtani is/are not necessary discuss about the carrier concentration of the second light shielding film because it would have been obvious to one having ordinary skill in the art at the time the invention was made that the carrier concentration of the second light-shielding film of Kawata and/or Ohtani can be chosen at various value(s), and at least one of such values can be in the range of $10^{17}/cm^3$ or less (since this is a wide range), since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233; or that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). See also paragraphs [0054-0069] of Ohtani.

Regarding claim 14, Kawata/Ohtani discloses the thin film transistor substrate further comprising pixel electrodes corresponding to each of said plurality of thin film transistors, wherein each of said pixel electrode is driven by a thin film transistor which said pixel electrode corresponds to. See fig. 3, 15 of Kawata, and/or figs. 8-10 of Ohtani.

Regarding claim 15, Kawata/Ohtani discloses the thin film transistor substrate wherein a dielectric film inbetween capacitance electrodes is connected to said pixel electrodes in parallel. See fig. 3, 15 of Kawata, and/or figs. 8-10 of Ohtani.

Regarding claim 16, Kawata/Ohtani discloses the thin film transistor substrate further comprising another thin film transistor (driver circuit) which comprises neither said first light-shielding film nor said second light-shielding film. See col. 13, line 7-28 of Kawata; and/or paragraph [0080] of Ohtani.

Regarding claim 17, Kawata/Ohtani discloses the thin film transistor substrate wherein an electric field intensity of a surface portion of said second light-shielding film which opposes said active layer includes about 80% or less of that of a surface portion of said second light-shielding film which opposes said first light-shielding film. It is noted that the surface portion of the second light-shielding film can obviously and varyingly be chosen, therefore the electric field intensity of the chosen portion can also be varied, and definitely be able to have value of about 80% or less of that of the surface portion of the second light shielding film.

Regarding claim 18, Kawata/Ohtani discloses the thin film transistor substrate wherein said second light-shielding film is made of a material selected from a group consisting of amorphous silicon, crystallite silicon, amorphous Silicon Germanium, poly germanium, amorphous germanium, poly Silicon Germanium, and any combination thereof. See col. 16, line 12 to col. 17, line 36; and col. 19, line 65 to col. 21, line 2 of Kawata; and/or paragraphs [0040]-[0044] of Ohtani.

Regarding claim 19, Kawata/Ohtani discloses a liquid crystal display unit comprising a thin film transistor substrate 10 (fig. 15 of Kawata) or 600 (fig. 9 of Ohtani) as claimed above; an opposite substrate 20 (Kawata) or 905 (Ohtani) disposed to oppose said thin film transistor substrate 10/600; and a liquid crystal layer disposed between said thin film transistor substrate and said opposite substrate.

Conclusion

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

Dao H. Nguyen
Art Unit 2818
November 9, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800